CLAIM AMENDMENTS

IN THE CLAIMS

This listing of the claims will replace all prior versions, and listing, of claims in the application or previous response to office action:

1. (**Currently Amended**) A circuit module comprising:

- a circuit board;

- multiple circuit units on the circuit board;

- at least one clock input on the circuit board for receiving an external clock signal;

- a first phase locked loop (PLL) unit on the circuit board for providing an internal clock signal based on the external clock signal to a first set of at least one of the circuit units; and

- a second PLL unit on the circuit board for providing an internal clock signal based on the external clock signal to a second set of at least one of the circuit units,

wherein **each circuit unit in the first set is connected to the first PLL unit and not to the second PLL unit and wherein each circuit unit in the** ~~**the**~~ second set **is connected to the second PLL unit and not to the first PLL unit** ~~**and the first set are mutually exclusive.**~~

2. (Original) The circuit module according to claim 1, wherein the circuit module is a memory module and wherein the circuit units are memory chips.

3. (Original) The circuit module according to claim 1, wherein each of the PLL units has a PLL clock input and wherein the PLL clock inputs of the PLL units are connected to different clock inputs on the circuit board.

4. (Original) The circuit module according to claim 1, wherein each of the PLL units has a PLL clock input and wherein the PLL clock inputs of the PLL units are connected to the same clock input on the circuit board.

5. (Original) The circuit module according to claim 1, wherein each of the PLL units has associated therewith a feedback loop designed to show a behavior similar to the behavior of a clock signal path between the PLL units and one of the circuit units, wherein the frequency of the internal clock signal is controlled based on a comparison of the external clock signal received at a PLL clock input of the PLL units and a version of the internal clock signal transmitted over the feedback loop.

6. (Original) The circuit module according to claim 5, wherein both PLL units share a common feedback loop in that a common portion of the feedback loop is connected to a feedback loop output of the first PLL unit and that the common portion branches into two feedback loop branches, wherein one of the feedback loop branches is connected to a feedback loop input of the first PLL unit and the other of the feedback loop branches is connected to a feedback loop input of the second PLL unit.

7. (Original) The circuit board unit according to claim 6, wherein the common portion branches into multiple feedback loop branches and wherein the number of the plurality of feedback loop branches corresponds to a number of circuit units connected to one PLL clock output of the PLL unit.

8. **(Currently Amended)** A memory module comprising:

- a circuit board;
- multiple memory chips on the circuit board;
- a clock input on the circuit board for receiving an external clock signal;
- a first phase locked loop (PLL) unit on the circuit board for providing an internal clock signal based on the external clock signal to a first set of at least one of the memory chips; and
- a second PLL unit on the circuit board for providing an internal clock signal based on the external clock signal to a second set of at least one of the memory chips,

wherein **each memory chip in the first set is connected to the first PLL unit and not to the second PLL unit and wherein each memory chip in the second set is**

connected to the second PLL unit and not to the first PLL unit~~**the second set and the first set are mutually exclusive.**~~

9. (Original) The memory module according to claim 8, wherein each of the PLL units has a PLL clock input and wherein the PLL clock inputs of the PLL units are connected to different clock inputs on the circuit board.

10. (Original) The memory module according to claim 8, wherein each of the PLL units has a PLL clock input and wherein the PLL clock inputs of the PLL units are connected to the same clock input on the circuit board.

11. (Original) The memory module according to claim 9, wherein each of the PLL units has associated therewith a feedback loop designed to show a behavior similar to the behavior of a clock signal path between the PLL units and one of the memory chips, wherein the frequency of the internal clock signal is controlled based on a comparison of the external clock signal received at a PLL clock input of the PLL units and a version of the internal clock signal transmitted over the feedback loop.

12. (Original) The circuit module according to claim 11, wherein both PLL units share a common feedback loop in that a common portion of the feedback loop is connected to a feedback loop output of the first PLL unit and that the common portion branches into two feedback loop branches, wherein one of the feedback loop branches is connected to a feedback loop input of the first PLL unit and the other of the feedback loop branches is connected to a feedback loop input of the second PLL unit.

13. (Original) The circuit board unit according to claim 12, wherein the common portion branches into multiple feedback loop branches and wherein the number of the plurality of feedback loop branches corresponds to a number of memory chips connected to one PLL clock output of the PLL unit.

14. **(Currently Amended)** A circuit module comprising:

- a circuit board;

- a plurality of memory chips arranged along the width of the circuit board comprising a first set of memory chips and a second set of memory chips;

- at least one clock input on the circuit board for receiving an external clock signal;

- a first phase locked loop (PLL) unit arranged within the first set of memory chips for providing an internal clock signal based on the external clock signal to a first set of at least one of the memory chips; and

- a second PLL unit arranged within said second set of memory chips for providing an internal clock signal based on the external clock signal to a second set of at least one of the memory chips,

wherein **each memory chip in the first set is connected to the first PLL unit and not to the second PLL unit and wherein each memory chip in the second set is connected to the second PLL unit and not to the first PLL unit**~~the second set and the first set are mutually exclusive.~~

15. (Original) The circuit module according to claim 14, wherein the first PLL unit is placed in an approximate geometrical center of said first set of memory chips.

16. (Original) The circuit module according to claim 14, wherein the second PLL unit is placed in an approximate geometrical center of said second set of memory chips.

17. (Original) The circuit module according to claim 14, wherein each of the PLL units has a PLL clock input and wherein the PLL clock inputs of the PLL units are connected to different clock inputs on the circuit board.

18. (Original) The circuit module according to claim 14, wherein each of the PLL units has a PLL clock input and wherein the PLL clock inputs of the PLL units are connected to the same clock input on the circuit board.

19. (Original) The circuit module according to claim 14, wherein each of the PLL units has associated therewith a feedback loop designed to show a behavior similar to the behavior of a clock signal path between the PLL units and one of the memory chips, wherein the frequency of the internal clock signal is controlled based on a comparison of the external clock signal received at a PLL clock input of the PLL units and a version of the internal clock signal transmitted over the feedback loop.

20. (Original) The circuit module according to claim 19, wherein both PLL units share a common feedback loop in that a common portion of the feedback loop is connected to a feedback loop output of the first PLL unit and that the common portion branches into two feedback loop branches, wherein one of the feedback loop branches is connected to a feedback loop input of the first PLL unit and the other of the feedback loop branches is connected to a feedback loop input of the second PLL unit.

21. (Original) The circuit board unit according to claim 20, wherein the common portion branches into multiple feedback loop branches and wherein the number of the plurality of feedback loop branches corresponds to a number of memory chips connected to one PLL clock output of the PLL unit.